

## **RADIOFREQUENCY DOUBLE POLE SINGLE THROW SWITCH**

### **RELATED APPLICATIONS**

[0001] This present application relates to commonly-assigned U.S. Patent Application  
5 Serial No. \_\_\_\_\_, filed July 7, 2003, Attorney Docket No 18054 (1110-03).

### **FIELD OF THE INVENTION**

[0002] This present invention relates to radiofrequency switches, and in particular, to  
microwave/millimeter wave switches.

### **BACKGROUND OF THE INVENTION**

10 [0003] Many applications require Double Pole Single Throw (DPST) switches that  
will direct one of two inputs to a single output upon the application of a particular control  
signal. Figure 1 shows a monopulse-type radar receiver 10, which is one example of an  
application which requires a DPST switch. The radar receiver 10 includes first and second  
reception antennae 20, 30 which are coupled to the two inputs of the DPST switch 50 through  
15 low-noise amplifiers (LNAs) 40, 45. The DPST switch 50 is used to select between one of  
the two reception antennae 20, 30, and thus select one of two received signals. The output of  
the DPST switch 50 is coupled to mixers 60, 65 which separate the received signal into in-  
phase (I) and quadrature phase (Q) components.

[0004] Conventionally, DPST switches operating at microwave and millimeter wave  
20 frequencies include complex networks based upon diodes and transmission lines than can be  
large and expensive.

[0005] Thus, there is presently a need for a DPST switch which operates at  
microwave and millimeter wave frequencies, but is small in size and inexpensive.

### **SUMMARY OF THE INVENTION**

25 [0006] An exemplary embodiment of the present invention comprises a switch circuit  
including a first circuit portion corresponding to a first input port, a second circuit portion  
corresponding to a second input port, and an output port, wherein each of the first and second  
circuit portions include at least one first transistor providing a portion of an isolation channel,  
at least one second transistor providing a portion of a transmit channel, and at least one third  
30 transistor for providing a control bias for selecting either the transmit channel or the isolation  
channel.

[0007] An exemplary embodiment of the present invention also comprises a method for providing isolation between at least two inputs and an output of a switch circuit including the steps of providing a first channel for each of the at least two inputs including at least one first differential amplifier pair, said first channel providing isolation between the at least two inputs and the output of the switch circuit, providing a second channel for each of the at least two inputs including at least one second differential amplifier pair, said second channel providing coupling between the input and output of the circuit, and providing a control bias which selects one of the at least two inputs and a respective first channel or second channel.

#### BRIEF DESCRIPTION OF THE DRAWINGS

[0008] Figure 1 shows a conventional monopulse-type radar receiver.

[0009] Figure 2(a) shows a Double Pole Single Throw switch circuit according to a first exemplary embodiment of the present invention.

[0010] Figure 2(b) shows the Double Pole Single Throw switch circuit of Figure 2(a) in more detail.

[0011] Figure 3 shows the switch circuit of Figure 2 implemented as an integrated circuit.

[0012] Figure 4 shows an enlarged view of the integrated circuit shown in Figure 3.

[0013] Figures 5(a)-5(i) are graphs showing a frequency versus decibel (dB) response for the switch circuit of Figure 2 in various states.

[0014] Figure 6 shows a schematic diagram of a conventional Gilbert Cell.

#### DETAILED DESCRIPTION

[0015] Embodiments of the present invention comprises a Double Pole Single Throw (DPST) switch which may be fabricated as an integrated circuit (IC).

[0016] One conventional technique for multiplying two signals together in an IC is through the use of a Gilbert Cell. As is well known in the art, a Gilbert Cell is typically implemented as a cross-coupled differential amplifier. Figure 6 shows an exemplary Gilbert Cell 100 which includes a first differential amplifier pair 110 (including transistors 111, 112),

and a second differential amplifier pair 120 (including transistors 121, 122). The collectors of transistors 111 and 121 are coupled to each other and to pin "5" of the Gilbert Cell 100. Similarly, the collectors of transistors 112 and 122 are coupled to each other and to pin "6" of the Gilbert Cell 100. Further, the bases of transistors 111 and 122 are coupled to each other and to pin "8" of the Gilbert Cell 100, and the bases of transistors 112 and 121 are coupled to each other and to pin "7" of the Gilbert Cell. Finally, the emitters of the transistors 111, 112 of the first differential amplifier pair 110 are coupled to the collector of a first bias transistor 130, and the emitters of the transistors 121, 122 of the second differential amplifier pair 120 are coupled to the collector of a second bias transistor 140. In operation, a differential AC bias voltage applied to the bases of the first and second bias transistors 130, 140 (through pins "1" and "4" of the Gilbert Cell) controls the amplitude of an input radiofrequency (RF) signal applied across pins "6" and "7" of the Gilbert Cell. As shown and described in the following figures, the present inventors propose various modifications of a Gilbert Cell so that it may be used as a DPST switch, as opposed to its traditional use as an amplifier.

**[0017]** Figure 2(a) shows a DPST switch circuit 200 according to a first exemplary embodiment of the present invention. The DPST switch circuit 200 includes a first input port 201, a second input port 202, and a first output port 203. The switch circuit 200 also includes a first switch section 205 corresponding to the first input port 201, and a second switch section 206 corresponding to the second input port 202. A control input port 207 provides a voltage signal controlling which of the switch sections 205, 206 are active (i.e., transmitting their signal to the output port 203).

**[0018]** The first switch section 205 includes transistors 240, 241', 245, 247, 250, 252, 254, and 256, and the second switch section 206 includes transistors 241, 240', 246, 248, 251, 253, 255, and 257. In operation, a control voltage is applied to control input port 207 such that the voltage applied to the base of either transistors 240 and 240' (Q8, Q16) or transistors 241 and 241' (Q7, Q15) is higher than the voltage applied to the other set of transistors by the thermal breakdown voltage of the transistors (e.g., 0.7 Volts(V)). For example, if the voltage applied to transistors 240, 240' is greater than the voltage applied to the transistors 241, 241', transistors 240, 240' are biased 'ON' and the first input port 201 'sees' a high input impedance, and thus the signal at the second input port 202 is transmitted to the output port 203. Similarly, if the voltage applied to transistors 241, 241' is greater than the voltage applied to the transistors 240, 240', transistors 241, 241' are biased 'ON' and the second

input port 202 'sees' a high input impedance, and thus the signal at the first input port 201 is transmitted to the output port 203.

[0019] In the case where first input port 201 is coupled to output port 203 (e.g., where transistors 240 and 240' are biased 'ON'), transistors 251 and 257 (Q11, Q12) are also biased 'ON' and transistors 246, 248, 253 and 255 (Q9, Q10, Q13, Q14) are biased 'OFF' so that the second section 206 doesn't load the output of the first switch section 205 at all, and all of the signal transmitted from the first input port 201 will appear at the output port 203.

Alternatively, in the case where second input port 202 is coupled to output port 203 (e.g., where transistors 241 and 241' are biased 'ON'), transistors 250 and 256 (Q1, Q2) are also biased 'ON' and transistors 245, 247, 252 and 254 (Q3, Q4, Q5, Q6) are biased 'OFF' so that the first section 205 doesn't load the output of the second switch section 206 at all, and all of the signal transmitted from the second input port 202 will appear at the output port 203.

Further details of the operation of the switch circuit 200 are discussed below with reference to Figure 2(b).

[0020] Figure 2(b) shows the DPST switch circuit 200 according to a first exemplary embodiment of the present invention in greater detail. Many of the elements shown in Figure 2(b) were also shown in Figure 2(a), and like reference numerals indicate like elements. As explained above, the DPST switch circuit 200 includes a first input port 201, a second input port 202, and a first output port 203. A supply voltage  $V_{dc}$  is provided to a network of transistor switches 208 (comprised of first section 205 and second section 206) coupled between the inputs 201, 202 and the output 203. Inductors 210, 211 provide isolation between the DC supply voltage  $V_{dc}$  and the AC voltage at the input ports 201, 202 and output port 203. Similarly, capacitors 215, 216 isolate DC voltages from the output port 203.

[0021] In accordance with the first exemplary embodiment of the present invention, a portion of the network of transistor switches 208 is laid out similarly to the above-described Gilbert Cell. In particular, the network includes bias transistors 240, 240', 241, and 241' (corresponding to bias transistors 130, 140 of the Gilbert Cell shown in Figure 14), interior transistors 245, 246 (corresponding to transistors 112, 121 of the Gilbert Cell shown in Figure 14), and exterior transistors 247, 248 (corresponding to transistors 111, 122 of the Gilbert Cell shown in Figure 14). However, instead of interior transistors 245, 246 having their bases coupled together they are decoupled. Further, additional transistors 250-257 are provided

around the 'modified' Gilbert Cell. For ease of illustration, not all of the biasing circuitry for each of the transistors 240, 240', 241, 241', 245-248 and 250-257 is shown in Figure 2(b).

[0022] Bias transistors 240 and 241', and 241 and 240', have their emitters coupled together and to a current source  $I_{dc}$ . The bases of the bias transistors 240, 240' are fed by a first voltage source  $V_{dc1}$  and the bases of bias transistors 241, 241' are fed by a second voltage source  $V_{dc2}$ .

[0023] It will be noted that transistor pairs 250/256, 245/247, 246/248, and 251/257 of the switch circuit 200 are all coupled in a 'cascode' configuration (i.e., emitter coupled). This cascode coupling of the transistors presents a high input impedance to each of the input ports 201 and 202. In particular, when input port 201 is applied to the output port 203, input port 202 presents a high input impedance, and when input port 202 is applied to the output port 203, input port 201 presents a high input impedance. The high input impedance prevents either of the unwanted ports (e.g., either input port 201 or 202) from loading the desired signal path. The cascode configuration of the transistor pairs 250/256, 245/247, 246/248, and 251/257 has little or no effect on the isolation between wanted and unwanted signals. It does, however, ensure that the wanted signal is directed to the output port 203 instead of being lost traveling to the other input port.

[0024] This high input impedance prevents extraneous signals from the unselected input port from being applied to the switch circuit 200.

[0025] Each of the two input ports 201, 202 is coupled to a separate portion of the network of transistors 208. For example, input port 201 is coupled to a first portion 205 including transistors 240, 241', 245, 247, 250, 252, 254 and 256, and input port 202 is coupled to a second portion 206 including transistors 240', 241, 246, 248, 251, 253, 255 and 257. Each of these first and second portions 205, 206 further include both a 'transmit' channel and an 'isolation' channel. For example, the 'transmit' channel for the first portion 205 (corresponding to input port 201) comprises transistors 245, 247, 252 and 254, and the 'isolation' channel comprises transistors 250 and 256. Similarly, the 'transmit' channel for the second portion 206 (corresponding to input port 202) comprises transistors 246, 248, 253 and 255, and the 'isolation' channel comprises transistors 251 and 257.

[0026] In operation, signals are applied to input ports 201 and 202, and either the input signal at port 201 or the input signal at port 202 is transmitted to the output port 203 at any given instant. The selection of which input port (e.g., 201 or 202) is applied to the output port 203 is accomplished by applying different voltages to the bases of bias transistors 240, 240', 241, and 241'. As will be understood by those skilled in the art, voltage sources  $V_{dc1}$  and  $V_{dc2}$  directly control the voltage applied to the respective bases of the bias transistor 240, 240', 241, and 241'. For example, if bias transistors 240 and 240' have a greater voltage applied thereto than bias transistors 241 and 241' (by at least approximately 0.7 volts, which is the thermal breakdown voltage of the bias transistors), input port 201 will be coupled to output port 203. Similarly, if bias transistors 241 and 241' have a greater voltage applied thereto than bias transistors 240 and 240' (by at least approximately 0.7 volts), input port 202 will be coupled to output port 203.

[0027] Figure 3 shows the switch circuit 200 of Figure 2 implemented monolithically. Figure 4 is an enlarged view of a portion of the monolithically-implemented switch circuit 200 showing the input ports 201, 202, and the output port 203 in greater detail.

[0028] Figures 5(a)-5(i) are graphs showing a frequency in GigaHertz (GHz) versus decibel (dB) response for the switch circuit 200 of Figure 2. In particular, Figures 5(a), (e) and (i) show input impedance matching curves for input ports 201 (Port 1), 202 (Port 2) and output port 203 (Port 3), respectively. The remaining figures show isolation curves for the switch circuit 200 as between different ports (e.g., Figure 5(b) shows an isolation curve between one of the input ports (Port 2) and another of the input ports (Port 1). As will be recognized by those skilled in the art, the isolation between the ports 201-203 of the switch circuit 200 is relatively uniform across the operational frequency range. As will be noted by those of ordinary skill in the art, the switch circuit 200 is always matched (i.e., the return loss of each port 201-203 stays constant irrespective of the switch's state).

[0029] Although the invention has been described in terms of exemplary embodiments, it is not limited thereto. Rather, the appended claims should be construed broadly to include other variants and embodiments of the invention which may be made by those skilled in the art without departing from the scope and range of equivalents of the invention.